B.S.T.J. BRIEFS

Planar Epitaxial Silicon Schottky Barrier Diodes

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It has been demonstrated that a metal-to-semiconductor rectifying junction can be designed as a fast computer diode.[1,2] It can also be designed as a high performance varactor.[3,4] There is increasing evidence that Schottky barrier diodes may, with suitable design modifications, outperform the conventional point contact diodes in the field of varistor applications.[5,6]

The earlier versions of ESBAR (Epitaxial Schottky Barrier) diodes had either a mesa-like structure, well-encapsulated to withstand the environmental influences, or a pseudo planar structure of doubtful passivation capability. Manufacturability of these diodes is greatly improved by taking advantage of the "planar" process of making diodes by the well-known photoresist masking. Such a structure is shown in Fig. 1.

The rectifying barrier in a planar ESBAR diode was obtained between a suitable metal having an appreciable amount of silicon in solution (for convenience, labeled as metal silicide in Fig. 1) and the epitaxial silicon. The metal silicide was formed by evaporating the metal over the silicon dioxide with appropriately sized windows, and allowing it to react with the exposed silicon at a suitable temperature (anywhere between 300°C and 700°C, depending on the metal used) for relatively short periods of about 30 minutes. The amount of Si depletion due to this solid-solid reaction can be controlled by the amount of metal available and the reaction temperature.

After removing unreacted metal by a suitable means, such as selective etching, which leaves silicon rich metal in the oxide window, a 0.5 μ thick Pt layer was deposited over the entire surface preceded by a thin film ($\sim$200 Å) deposition of Cr or Ti. The latter metals insure good adhesion of Pt layer on the oxide surface inhibiting lateral diffusion of ambient gases. The photoresist technique was again used to achieve a selective Au plating on Pt, overlapping the oxide window. The thickness of this plated Au is typically a few microns. This serves as an effective mask for the operation of Pt removal by some means,

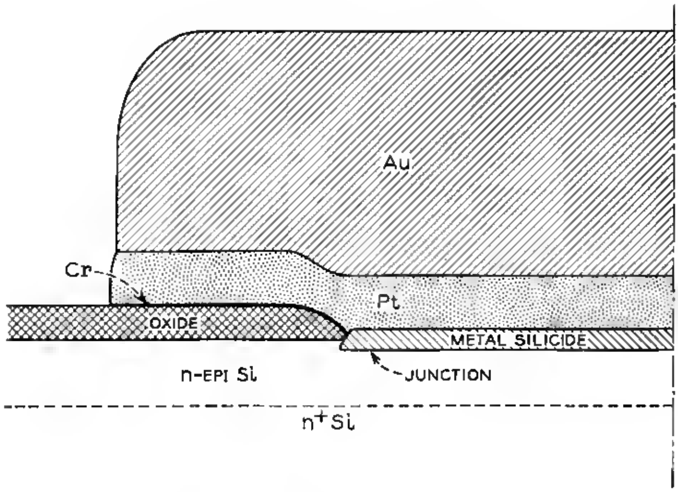

Fig. 1 — Structure of planar ESBAR.

such as backsputtering,[7] from surfaces other than the ones under the Au layer.

The major feature of this structure is the reasonable passivation of the rectifying barrier against the environment and suppression of leakage currents. For instance, the leakage current is much smaller in these diodes than the mesa type diodes. The n factor in the diode equation

$$I = I_s \exp\left(\frac{qV}{nkT} - 1\right)$$

is less than 1.1 as compared to 1.2–1.5 for the unprotected diodes of area of one mil diameter circle. Forward characteristics of Cu-Si diodes of diameter of 2, 1 and $\frac{1}{2}$ mils are shown in Fig. 2. Here $n =$ 1.03, the theoretically expected value.[8] Sharp reverse breakdown is common for these diodes as opposed to the mesa type where it is a rarity.

These diodes, unencapsulated, have shown no degradation after 100 hours aging at 350°C in room air or at 300°C in one atmosphere of steam. As for the non-planar diodes, hermetically sealed encapsulation is mandatory in order to survive such stress agings.

The barrier height measured from the Fermi level of a metal silicide diode is significantly different from the metal-silicon barrier height. For instance, a Pt-Si diode has barrier height of larger than 1 volt while a Pt silicide-Si diode has the value of 0.87 volt. Cu-Si system

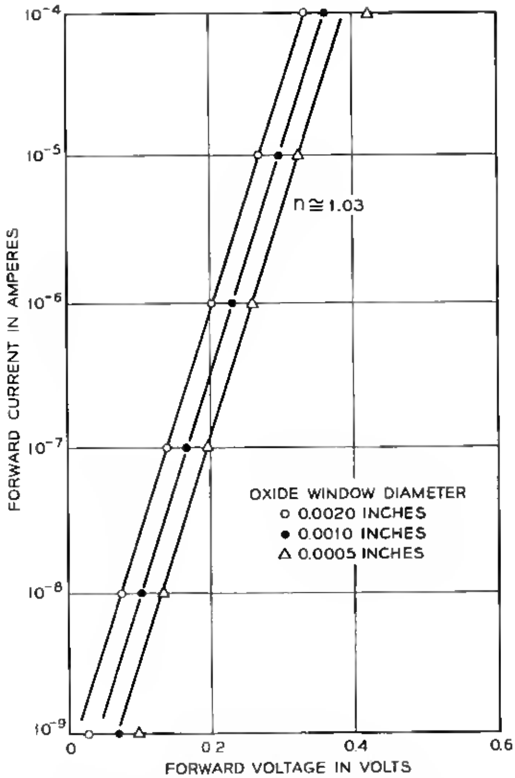

Fig. 2 — Forward characteristics of planar copper silicide, epitaxial silicon, surface barrier diodes.

gives the barrier height of 0.58 volt. Cu-Silicide-Si system, after 30 minutes heating at 350°C, has the barrier height of ~0.78 volts. If more Si is allowed to dissolve in the "silicide", by raising the reaction temperature, the barrier height increases to saturate at about 0.9 volts. This saturation occurs at various temperatures depending on the metals. For instance, Mo-Si barrier shows little change after heating up to 700°C. Similar results on W-Si system have also been reported.[9]

In addition to increased reliability, one obtains with the planar ESBAR structure, better control of diode geometry inherent with the photoresist techniques. This should result in much more uniform terminal characteristics of the diodes. One of the important parameters is the stray capacitance associated with the Pt overlay. One wishes, in general, to minimize the stray capacitance. It should be recognized

that minimization of the stray capacitance associated with the overlay is achieved only with decreased ambient protection due to the decrease in the overlay area.

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4-gc Transmission Degradation Due to Rain at the Andover, Maine, Satellite Station

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I. INTRODUCTION

The microwave link between a ground station and a communications satellite is normally very stable and essentially free from fading. Under conditions of rain or snow, however, the transmitted and received signals encounter extra attenuation and additional noise is introduced into the low-noise receiver on the ground. A good knowledge of such rain effects is important for the design of satellite ground stations which have to meet certain statistical requirements for transmission degradation. It is known that radome covered ground stations like Andover, suffer more degradation during rain than uncovered stations. Some analytical work has been done by D. Gibble[1] and B. C. Blevis[2] to determine the effects of a water layer on radomes. Their theoretical work has been supplemented by an experimental technique applicable at existing satellite ground stations and to be described in this brief report. It consists of measuring the reduction of the noise power received from the strong and stable radio star Cassiopeia A during periods of rain.